Microshutter Arrays for Near-Infrared Applications On the James Webb Space Telescope

M. J. Li[*1], A. Bier[1, 2], R. K. Fettig [1,3], D. Franz[1, 3], R. Hu[1, 3], T. King[1], A. S. Kutyrev[1, 3], B. A. Lynch [1,3], S. H. Moseley[1], D. B. Mott[1], D. Rapchun[1, 3], R.F. Silverberg[1], W. Smith [1,4], L. Wang[1, 5], Yun Zheng [1,6], C. Zinke[1, 6]

[1]NASA Goddard Space Flight Center, Greenbelt, MD 20771, USA
[2]Global Science and Technology, Greenbelt, MD 20771, USA
[3]Raytheon Corp. ITSS, Lanham, MD 20770, USA
[4]Orbital Science Corp. ITSS, Lanham, MD 20770, USA
[5] Swales Aerospace Co., Greenbelt, MD 20705, USA
[6] QSS Group, Inc., Lanham, MD 20770, USA

ABSTRACT

Magnetically actuated MEMS microshutter arrays are being developed at NASA Goddard Space Flight Center for use in the near-infrared region on the James Webb Space Telescope (JWST), formally Next Generation Space Telescope (NGST). The microshutter arrays are designed for the selective transmission of light with high efficiency and high contrast. The JWST environment requires cryogenic operation at 45K. Microshutter arrays are fabricated out of silicon-oxide-insulated (SOI) silicon wafers. Arrays are close-packed silicon nitride membranes with an original pixel size of 100x100 μm and 100x200μm for a new design. Individual shutters are patterned with a torsion flexure permitting shutters to open 90 degrees with a minimized mechanical stress concentration. The mechanical shutter arrays are fabricated using MEMS technologies. The processing includes a multi-layer metal deposition and patterning of shutter electrodes and magnetic pads, reactive ion etching (RIE) of the front side to form shutters out of the nitride membrane, an anisotropic back-etch for wafer thinning, and a deep RIE (DRIE) back-etch down to the nitride shutter membrane to form support frames and relieve shutters from the silicon substrate. An additional metal deposition and patterning is recently developed to form vertical electrodes. Shutters are actuated using a magnetic force and latched using an electrostatic force. 1D addressing was demonstrated. Shutters survived fatigue life tests.

KEYWORDS: microshutter, magnetic actuation, MEMS, RIE, DRIE, micro-optics, near-infrared, space telescope

1. INTRODUCTION

Energized by rapid growth of Micro-Electro-Mechanical-System (MEMS) technologies, multiple MEMS devices are being developed at NASA Goddard Space Flight Center (GSFC) for both space science and earth science applications. Typical MEMS devices are microshutter arrays, micromirror arrays, RF-MEMS switches, mass spectroscopes, Fabry-Pero filters, etc., in various development stages. Microshutter arrays are developed for a space science application, the James Webb Space Telescope (JWST), formally Next Generation Space Telescope (NGST), in the near-infrared (NIR) region.

1.1 Background

The primary mission of JWST is to reveal the origins of galaxies, clusters, and large-scale structures in the universe. In order to observe galaxies at the peak of the merging and star-forming era, JWST operation requires a spectroscopic coverage in the NIR wavelength region from 0.6 to 5 μm. A Multi-Object Spectrometer (MOS) is proposed for JWST to

[*] mary.j.li.1@gafc.nasa.gov, phone 301-286-9921, fax 301-286-1672; Code 553, Goddard Space Flight Center, Greenbelt, MD, USA 20771

fulfill the detection of the NIR[1]. An object selector is needed for the MOS to increase instrument observing efficiency by optimally filling the focal plane without spectral overlap. The primary requirements for the selector include: a >1800 x >1800 square element array (scaled appropriately if rectangular elements are used) with an element size (currently switching from 100 μm x 100 μm to 100 μm x 200 μm in our case) to cover the large JWST field of view, a fill factor on the order of 80% or better, contrast >2000, and operation in a cryogenic (around 45 K) environment to assure negligible thermal emission into the spectrometer.

Among MEMS candidates for the object selector for the MOS on JWST[2,3] were microshutter array technology and two micromirror array technologies, as developed by GSFC and Sandia National Laboratories. The disadvantage of using a micromirror array as an object selector is that micromirrors are reflective devices and they diffract and scatter light and therefore provide low contrast. Using the microshutter array technology, individual elements can be actuated to be fully open, allowing light to pass through. Microshutter devices have the potential to achieve higher contrast than reflective devices. In January, 2002, the microshutter array technology was selected as the MEMS candidate for the object selector for the MOS on JWST.

1.2 Original Design And Fabrication Of Microshutter Arrays

An original design of microshutters consists 100x100 μm unit cells. Microshutters are connected to a frame through a neck region and a torsion beam, as shown in Figure 1. Shutters open 90 degree out of plane through a shutter tilt along the axis of the torsion beam. In previous work, material selection for shutters was carried out through a series of mechanical testing and numerical analyses[4,5]. In addition, mechanical responses of torsion beams were studied to optimize their physical sizes and geometry[5] and shutter array actuation mechanisms were developed and demonstrated using prototype devices with the goal of achieving fully programmable addressing and maximizing fill-factor[5,6].

The shutters and torsion beams are 0.5 μm-thick silicon nitride. As shown in Figure 1, single crystal silicon grids, 100 μm-thick, with wall thickness of 8 μm or less, support the silicon nitride frame of the shutter array. Around the perimeter of the shutter cell will be an overhanging light shield. This shield blocks light from leaking through the gaps between shutters and hinges and the array frame when the shutters are in the horizontal closed position. On the structure of the shutter and frame are two sets of strip electrodes used for addressing the array, column electrodes and row electrodes. The design and the function of the electrodes were discussed in detail in a previous paper[8]. Deposited over the column electrodes on the shutters is a region of magnetic Co(90)Fe(10) alloy. This allows the shutters to be actuated by an external magnetic field. In the configuration intended for the JWST MOS, a linear magnet aligned to the shutter rows is swept across the array along the columns. As the magnet sweeps across the array, sequential rows of shutters are rotated from their natural horizontal closed orientation to a vertical open orientation in contact with the vertical electrodes. If the electrodes are voltage-biased to provide enough electrostatic force to overcome the mechanical restoring force of the torsion beam, the shutters will remain attached to the vertical electrodes in their open state. If the bias is insufficient, the shutters will return to their horizontal neutral closed position.

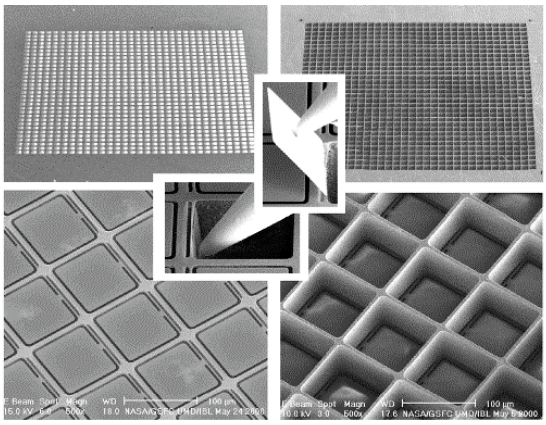
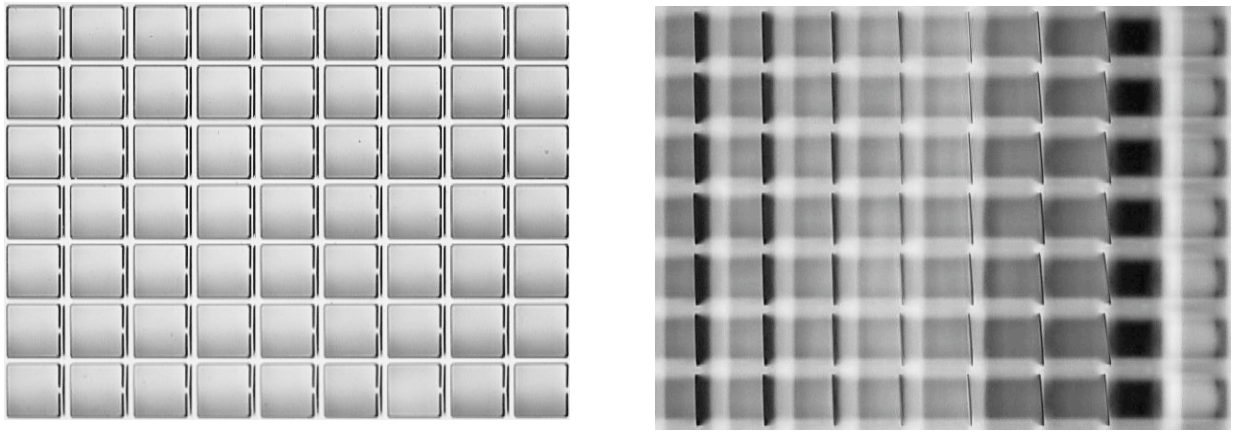


Figure 1: SEM images of the front side and backside of a 32x32 microshutter array with zoom-in images of a single shutter cell.

Microshutter array fabrication is carried out through conventional semiconductor processing and MEMS techniques. Shutter arrays with 32x32 and 128x128 pixels are fabricated out of silicon-oxide-insulated (SOI) silicon wafers. The processing includes a multi-layer metal deposition and patterning of shutter column electrodes and magnetic pads, a reactive ion etching (RIE) on the front side to form shutters out of the nitride membrane, an anisotropic back-etch for wafer thinning, followed by a deep RIE (DRIE) back-etch down to the nitride shutter membrane to form frames and

relieve shutters from the silicon substrate. An additional metal deposition and patterning has been developed to form vertical electrodes in rows. The fabrication of each component was described in detail in previous papers[7,8]. Thermal stress introduced by the intrinsic stress of deposition and the mismatch of thermal expansion coefficients between metal films and silicon nitride and related tests were also discussed in the papers.

Magnetic actuation of 128x128 microshutter array was demonstrated and published in previous work[7,8]. Figure 2 shows optical images of shutters (a) all closed (no magnet), and (b) a spectrum of open positions with the linear magnet under the array. The dark areas shown in Figure 2(b) are the sides of shutters opening at different angles due to the spatial variation in the magnetic field. The image indicated that the magnet for shutter actuation was moved to the position underneath shutters in the third column from right where shutters opened 90 degrees out of plane. The microscope was focused on the open edge of the shutter blades, but due to the small depth of field at this magnification, the shutter array frame is out of focus. The test array shown in figure 2 was intended for tests of the magnetic material and does not have addressing electrodes.



(a) (b)

Figure 2. Shutter arrays with Co(90)Fe(10) magnetic coating, (a) closed shutters, and (b) actuated shutters showing open shutter image (dark) with focus on top edges

The work presented in this paper is again primarily focused on the fabrication of the microshutter arrays. After the demonstration of the magnetic actuation, our new focus is electrostatic addressing of shutters. The goal is activating and addressing individual shutters within the array. Meanwhile, the requirement of a high fill factor imposes tight tolerances on the shutter frame dimensions. In order to meet the requirement we have modified fabrication procedures by moving previously designed cryogenic CMOS drive electronics off the shutter frames within the array on to the substrate. The modification leaves only necessary components, the strip shutter electrodes, on the shutter frame, which minimizes the width of the shutter frame to 8 μm or less. With newly designed and fabricated shutter electrodes and a single blanket vertical electrode we demonstrated 1D addressing. We are working on the delineation of vertical electrodes to demonstrate 2D addressing. In order to further increase the fill factor, we have been working towards the fabrication of 32x16, 128x64 and 512x256 microshutter arrays with a pixel size of 100x200 μm. Light shield development and the integration of light shield into the shutter wafer fabrication will be our next milestone following the 2D addressing.

2. RECENT DEVELOPMENT OF MICROSHUTTER ARRAYS

In recent development of microshutter arrays, our milestones are the 1D shutter line addressing, followed by the 2D individual shutter addressing. Since the shutters are addressed electrostatically as described in previous work[8], we have been refining the fabrication of the strip electrodes including column electrodes, also called shutter electrodes, and row electrodes, also called vertical electrodes. The shutter electrodes are fabricated on the front side of shutter arrays, while the vertical electrodes on the backside of the arrays, i.e. the side of the grid.

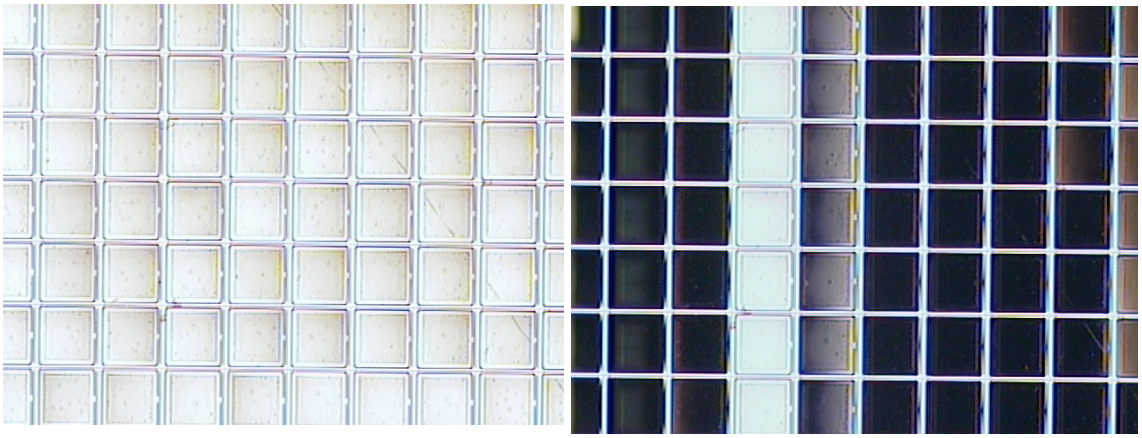
2.1 The 1D Addressing of Shutter Arrays

The 1D addressing, allowing addressing of lines of shutters, requires delineated shutter electrodes and a single blanket vertical electrode. We have fabricated 128x128 shutter arrays with re-designed shutter electrodes and the single blanket vertical electrode. As shown in Figure 3, a 200nm thick shutter electrode metal layer is delineated to columns. The shutter electrode on each column covers all shutters, torsion beams, and the shutter frame within the column. The square Co-Fe magnetic pads are patterned over the electrode metal layer on the shutters. We have used Aluminum and gold as the shutter electrode metal, respectively. A 15 nm-thick chromium is coated between the gold film and shutters as a barrier layer. The intention of using gold was to accommodate two later fabrication steps, the gold electrode pad etching by combining the shutter electrode etch and the electrode pad etch to one, and the silicon oxide etching by avoiding the oxide etching solution attacking. Both steps are carried out through wet etching. It was found that there are disadvantages for using gold as the shutter electrode metal. It is difficult to control Au-etch uniformity because the etch covers both the shutter area with small features as 2 μm-wide gaps and the electrode pad area that requires large-area etching as hundreds of μm. The gold electrode pads are located on the outer frame of the shutter array for connecting the shutter electrodes to a substrate through a flip chip bonding process. Another issue was raised during magnetic actuation testing for the shutters. It is difficult to actuate shutters with gold shutter electrodes. It is under investigation whether gold promotes Co-Fe oxidation or the combination of gold and Co-Fe weakens the ferromagnetic property of the magnetic pads through diffusion or other mechanisms.

Figure 3. An area of a shutter array with shutter electrodes in columns and Co-Fe magnetic pads over shutters for actuation

Figure 4. An area of the backside of a shutter array with a single blanket vertical electrode covering surface of silicon frame and one side of the frame walls

The fabrication of the vertical electrode is carried out through two-step angle depositions. Applying a DRIE etch, the 100 μm-thick silicon substrate underneath the shutter membranes is etched through from the backside of the wafer forming the silicon frame supporting the shutter membranes. In order to provide enough insulation between the shutter electrodes on the front side of the array and the vertical electrodes on the backside of the array, 150nm-thick Al_2O_3 is deposited on the surface of the silicon frame and one side of the shutter window walls by angle depositions. This portion



(a) (b)

Figure 5. Optical images for 1D addressing of a microshutter array demonstrated the line-addressing capability, (a) before and (b) after actuation

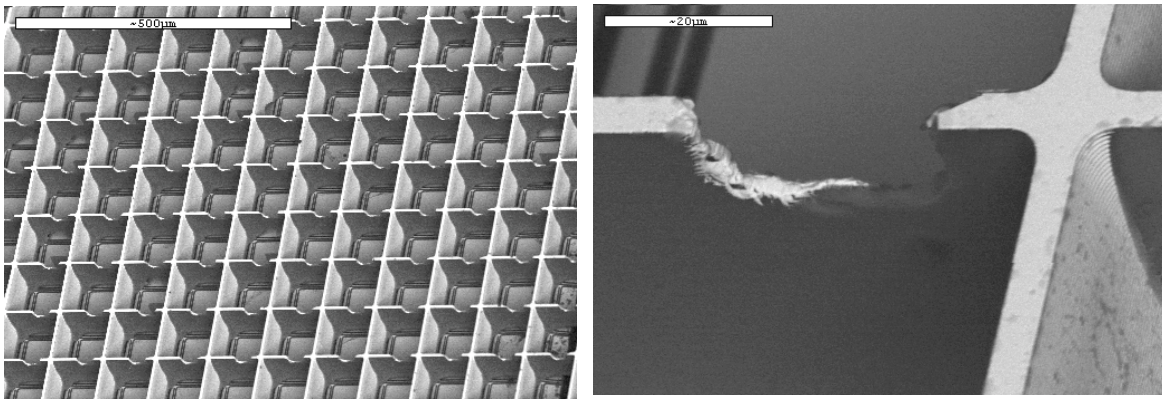
of the walls is on the side of torsion beams of shutters because the vertical electrode has to be made on this side for shutter latching when the shutters are opened in a shutter addressing process. The deposition angle is controlled to obtain a depth of 70 μm Al_2O_3 into the silicon windows. A wafer holder was made for the Al_2O_3 deposition with a water-cooling system and with functions of both wafer tilting and rotation. Following the Al_2O_3 deposition are the second-step angle depositions of vertical electrode metals. 15 nm-thick chromium and 500 nm-thick gold are deposited with an angle to obtain a depth of 60 μm metals into the windows.

The 1D addressing was demonstrated using the fabricated shutter arrays. As comparison, Figure 5(a) shows a close-up of a shutter array with delineated shutter electrodes and a single blanket vertical electrode, allowing the 1D addressing of lines of shutters. Figure 5(b) shows the same area with shutter lines addressed selectively. The entire 128x128 array was mounted on a silicon substrate through a flip chip bonding process. The substrate is made with an opening in the center and in the size of the shutter array to allow light to pass through. The critical voltage for latching was found to be on the order of 25 V. Due to limitations in our current electronics, only 32 columns and 32 rows were addressed at this time. 128x128 electronics are being developed. The current drive electronics and future bench-top test electronics will be based on off-the-shelf electronic components, while the JWST flight system will be driven by custom cryogenic CMOS circuits.

Since shutter electrode metal is also coated on torsion beams, it is necessary to conduct mechanical tests to estimate the fatigue life of the shutters. Bulk aluminum fails at low cycle fatigue within hundreds or thousands of cycles when the stain level is high. Aluminum on the torsion beams of the shutters experiences the maximum strain of ? when the shutters are fully open. However the shutters survived 10 million cycles at a cycling rate of 20 cycles per second without aluminum fatigue. This interesting result is probably due to the grain size of thin-film aluminum being much smaller than bulk aluminum..

2.2 Vertical Electrode Development For the 2-D Addressing

In comparison to the 1D addressing, the delineation of the vertical electrodes is also required besides that of the shutter electrodes for the 2D addressing. It is a challenging task to pattern the vertical electrodes on a silicon grid with 100 μm-deep shutter windows and a few μm-wide vertical frame walls. We have put efforts on various patterning techniques including photoresist spinning, spraying, dipping, and laminating, mechanical dicing, and shadow masking. It was found that the last two techniques provide better results in terms of good uniformity of patterning, high electrical insulation between delineated vertical electrodes, and also high electrical insulation between the shutter electrodes on the front side of a shutter array and the vertical electrodes on the backside of the array.



(a) (b)

Figure 6. (a) Vertical electrodes delineated by mechanical dicing, and (b) a diced groove and the portion of the groove that was blocked from metal deposition

The mechanical dicing is applied after the DRIE of shutter arrays and before the two-step angle depositions of Al_2O_3 and vertical electrode metals. The silicon frame is diced to obtain grooves that are perpendicular to the shutter electrode columns using an ultra-thin dicing saw. The grooves are diced out with a width controlled within 20 μm and a depth

between 20 μm to 25μm. The dicing lines are aligned close to the frame walls opposite to the torsion beams and the grooves are diced deep enough so that no metals are able to get into a particular portion of the grooves during the angle depositions. It is the blocking of metal deposition that fulfills the delineation of the vertical electrodes. After the mechanical dicing, shutter arrays are processed through the two-step angle depositions as described in Session 2.1. Figure 6 shows (a) vertical electrodes delineated by mechanical dicing, and (b) a close-up of a diced groove and the portion of the groove that is blocked from the metal deposition.

An alternative approach to the vertical electrode deposition is the shadow masking technique. The first step is to make shadow masks. We utilize the micromachining technologies for the fabrication of the shadow masks out of 4-inch SOI silicon wafers. The silicon on the device side of the wafer is 100μm-thick and that on the substrate side 400 μm-thick. The processing involves a DRIE etch to form 16mm-long, 27μm-wide, and 100μm-thick silicon strings, a silicon oxide growth to protect the strings from wet etching, an anisotropic silicon wet etch to etch through the substrate in order to open windows for the silicon strings, and a silicon oxide etch to remove the buried oxide layer and release the silicon strings. Traditional shadow masks are made from metals such as stainless steel and Invar alloy. Patterned features are laser-drilled, which introduces metal deformation leading poor flatness. Comparing metal shadow masks, silicon shadow masks provide very high flatness due to the high elastic limit of silicon. Taking the advantage of micromachining, silicon shadow masks also allow patterning intricate features such as small features of μm scale and those with high aspect ratios. Figure 7 shows a SOI wafer containing shadow masks for the deposition of the vertical electrodes for six 128x128 shutter arrays. These shadow masks achieve an aspect ratio above 160:1 without deformation.

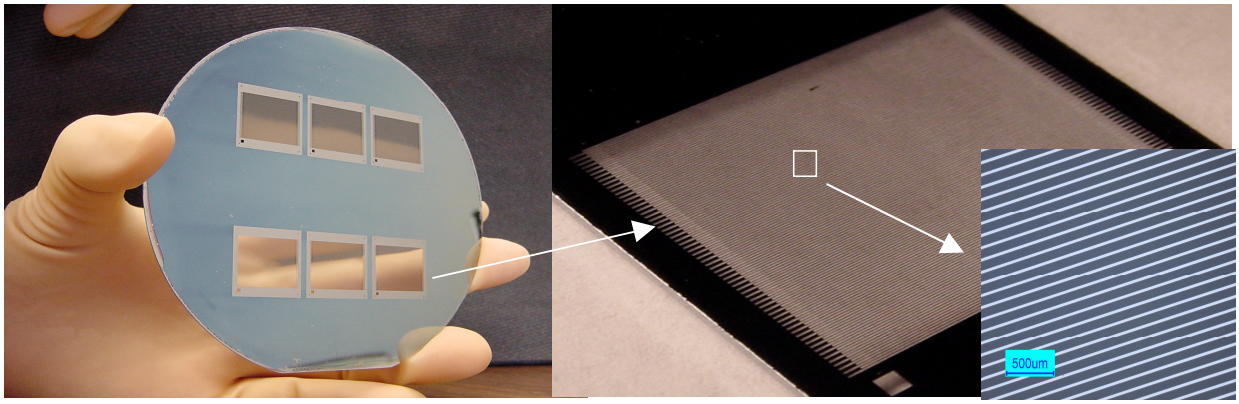


Figure 7. Shadow masks for vertical electrode deposition. The images show a SOI wafer with 6 shadow masks for 128x128 arrays, a close up of one of the shadow masks, and a close up of shadow mask strings.

Similar to the mechanical dicing technique, Al_2O_3 and metals are deposited with different angles to obtain different depth of the vertical electrode into shutter windows. Shadow masks are used only for the metal deposition. Figure 8 shows the vertical electrodes deposited on a 128x128 shutter array. It is important to deposit the metals, chromium and gold, covering a half of the frame surface in order to delineate the vertical electrode completely. The alignment between the shadow mask and the shutter array is achieved using a mask aligner. Due to the angle deposition, a tight attachment between the shadow mask and the shutter array is required. A gap between the two may lead to metal leaking into the shutter windows, which may affect the releasing of shutters from the frame.

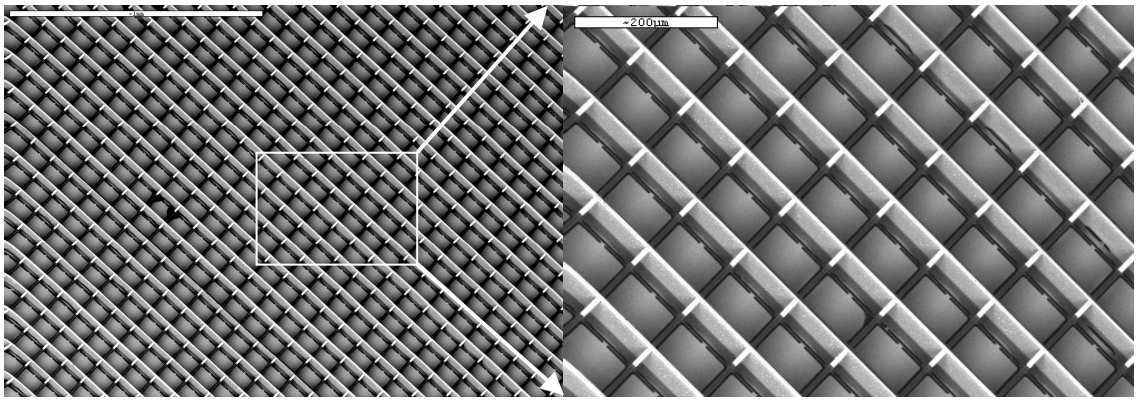


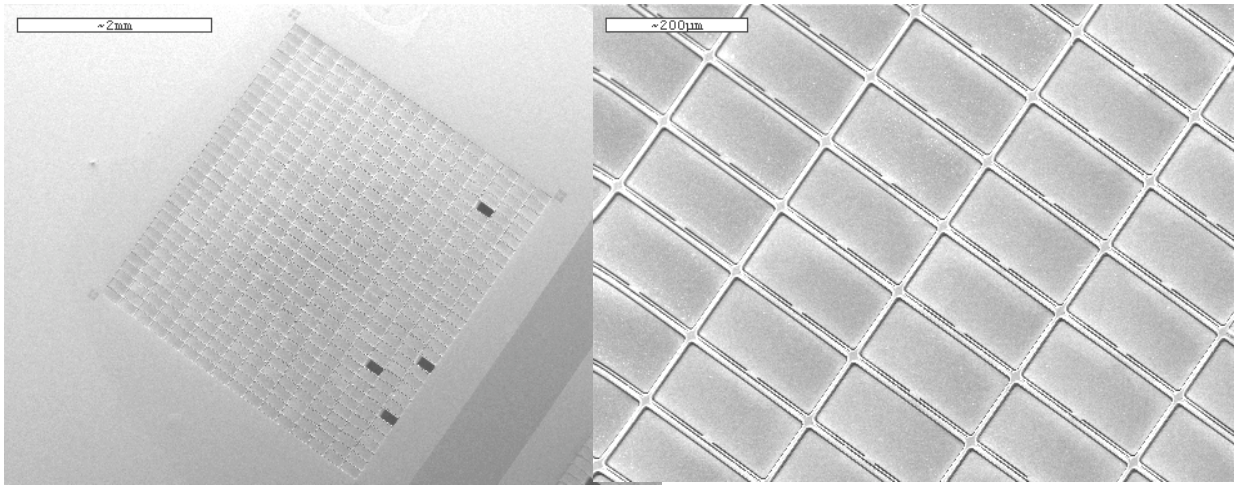
Figure 8. Vertical electrodes of a shutter array fabricated using the shadow masking technique

Comparing the mechanical dicing and the shadow masking techniques, both of the techniques require a flat surface of shutter arrays, which allows a uniform mechanical dicing depth and prevents a metal leak for the shadow masking. The mechanical dicing is simple and straightforward, while the shadow masking requires the shadow mask fabrication but no damage to the shutter arrays.

We continue to improve the fabrication of the vertical electrodes of shutter arrays towards the milestone of 2D addressing. There is an alternative method possibly for both the mechanical dicing and the shadow masking. One is "mechanical" DRIE-etching. Prior to the DRIE for shutter windows, an extra DRIE etching could be applied to make the "grooves" instead of saw dicing. The "grooves" could play the same role as those in the mechanical dicing by blocking metal deposition in certain areas in order to delineate the vertical electrodes. The second is "shadow masking on wafer". Similar to silicon shadow masks, shadow mask strings could be made of photoresist or other organic materials and patterned on the wafer. The patterning could be processed after the patterning for DIRE etching but prior to the DRIE etching itself towards the milestone of 2D addressing.

2.3 From 100x100 μm pixel Size to 100x200 μm pixel size

Once we reach the goal of the 2D addressing, we will develop light shield on shutter frames to improve contrast. The next goal will be the integration of the light shield into the fabrication of 128x64 shutter arrays with a pixel size of 100x200 μm. Larger shutter cells are being investigated for not only improvements in fill factor but also reduction in operating voltage. The larger shutter cell size improves the fill factor since most of the losses are those around the perimeter of the cell due to the frame and light shield. Total perimeter length reduces as the cell size increases, resulting in an improvement in fill factor. The operating voltage decreases as the cell size increases since the electrode area increases and the torsion hinges become less stiff as they increase in length.



(a) (b)

Figure 9. (a) A 32x16 shutter array with a pixel size of 100x200 μm and (b) a close-up image

We have fabricated 32x16 mechanical arrays with the pixel size of 100x200μm. The total area of the array is the same as that of 32x32 shutter arrays with a 100x100μm pixel size, while the total perimeter around shutters is reduced about a quarter in length. The total area of the shutter frame and the light shield may be reduced about 20%. The large-size shutters look mechanically robust through the processing so far. Thermal stress introduced by the in intrinsic stress of deposition and the mismatch of thermal expansion coefficient between the triple metal layers and the silicon nitride thin

films may cause shutters bowing. The effect of metal thickness, magnetic pad sizes and geometry on thermal stresses is under investigation. Optical tests and magnetic actuation tests will follow to evaluate the large-size shutters.

3. SUMMARY AND FUTURE WORK

Microshutter arrays are designed as an object selector for the Multi-Object Spectrometer on the James Webb Space Telescope. Microshutter arrays are transmissive devices minimizing light scattering to provide the high contrast needed for spectroscopy. We have fabricated 32x32 and 128x128 mechanical microshutter arrays with 100x100 μm pixels, and 32x16 mechanical arrays with 100x200 μm pixels, using combined conventional semiconductor processing and MEMS technologies. Materials for shutter membranes, oxide etch-stop, magnetic pads, electrodes and bonding pads have been tested and selected. We have used a combined magnetic and electrostatic approach for actuation and addressing. We successfully demonstrated cyclic fatigue tests and the 1D addressing. We are working on the fabrication of microshutter arrays with vertical electrodes for the 2D addressing.

Our goal is to fabricate 512x256 microshutter arrays in a 100x200μm pixel size with full actuation and addressing functions. We plan to develop 2048x1024 microshutter arrays as a mosaic of 16 512x256 arrays with a mechanical support and electrical interconnect frame between the arrays. Functional testing will be carried out in a cryogenic environment in the near future.

ACKNOWLEDGEMENTS

The microshutter project is supported by grant from NRA98-GSFC-1, NRA98-OSS-10, NRA99-OSS-05, and NRA00-OSS-03. We express our appreciation to Scott Schwinger for his magnet actuation stage design, Jonathan Kuhn and Jim Laughlin for their numerical analysis, and colleagues at NRL, especially Shu-Fan Cheng, for magnetic materials testing and deposition.

REFERENCES

[1] H. Stockman, the Next Generation Space Telescope: *visiting a time when galaxies were young,* The association of Universities for Research in Astronomy, Inc., 1997.
[2] J. MacKenty and M. Stiavelli, "A Multi-object Spectrometer Using Micro Mirror Arrays," in IMAGING THE UNIVERSE IN THREE DEMENSIONS: Astrophysics With Advanced Multi-Wavelength Imaging Devices, W. van Breugel and J. Bland-Hawthorn, eds., ASP Conference Series, 1999.
[3] D. J. Garcia and Nichols, "Silicon Micromirrors for the Next Generation Space Telescope," American Astronomical Society Meeting 196, pp. 2304+, May, 2000.
[4] J. Kuhn, R. Fettig, S. Moseley, A. Kutyrev, and J. Orloff, "Fracture Tests of Etched Components using a Focused Ion Beam Machine," Proceedings of SPIE4180, 2000.
[5] F. Fettig, S. Moseley, A. Kutyrev, J. Orloff, J. Kuhn, and L. Shude, "Some Aspects on the Mechanical Analysis of Micro-shutters," in Materials and Device Characterization in Micromachining II, Proceedings of SPIE 3875, 1999.
[6] S. H. Moseley, R. K. Fettig, A. S. Kutyrev, M. J. Li, D. B. Mott and B.E. Woodgate, "Status of the Development of 128x128 Microshutter Array," in MOEMS and Miniaturized Systems, Proceedings of SPIE 4178, 2000.
[7]Li, M.J.;, I. S.Aslam, S.I.; Ewin, A.; Fettig, R.K.; Franz, D. ; Kotecki, C. , Kutyrev, A.S.; Moseley, S.H.; Monroy, C ; Mott, D.B.; Zheng, Y., "Fabrication of Microshutter Arrays for Space Application", in Microelectronic and MEMS Technologies, Proceeding of SPIE, 2001.
[8]Mott, D.B.; Aslam, S.; Blumenstock, K.A.; Fettig, R.K.; Franz, D.E.; Kutyrev, A.S.; Li, M.J.; Harvey Moseley, S.H.; Monroy, C.J.; Schwinger, D.S. " Magnetically Actuated Microshutter Arrays", in Micro-machining and Microfabrication, Proceeding of SPIE, 2001.